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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/371,955	08/11/1999	SHANE P. LEIPHART	M4065.0196/P	9847

7590 01/02/2002

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EXAMINER
KANG, DONGHEE

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/371,955	LEIPHART, SHANE P.	
	Examin r	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Prosecution Application

1. The request filed on September 18, 2001 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/371,955 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **26-32 & 37-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al (US 5,313,101) in view of Kanamori (US 5,281,850).

Regarding claims **26-32**, Harada et al discloses a semiconductor device comprising (Fig.2G):

a memory circuit region in a semiconductor substrate; a first dielectric layer (3); an aluminum layer (4) over the dielectric layer; a contact interconnect between the aluminum layer (4) and substrate (1); a second dielectric layer (5) on the aluminum layer; a via hole extending through the second dielectric layer to aluminum layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium compound layer (102) formed on the titanium aluminide; a conductive material (103') formed on the titanium nitride layer; and a second metallic layer (103) on the second

dielectric layer and electrically connected to the plug material. Harada does not teach a *preformed* titanium aluminide. The term "*preformed*" is process limitation which recites process step to form the structure claimed in 26-28. The process limitation is given no patentable weight in device claim. The final structure of claimed invention is identical to the Harada's device. Therefore, claimed structure is taken to be in the least obvious over Ichikawa.

If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior the prior product was made by a different process". In re Thorpe, 777F. 2d 695,698 USPQ 964, 966 (Fed. Cir. 1985). See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Harada et al does not teach an antireflecting coating layer over the aluminum layer.

However, Kanamori teaches in Fig.1(f) the antireflecting coating layer (5) located at between aluminum layer and second dielectric layer. It is common to use a layer of material to suppress reflections from underlying surfaces during photolithography exposure steps. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the antireflecting coating layer, since antireflecting coating layer suppresses reflections from underlying layers so that the photoresist is not exposed to the reflected light wave, which leads to variation in critical dimensions.

Regarding claims **37-40**, Harada et al discloses a semiconductor device comprising (Fig.2G):

a memory circuit region in a semiconductor substrate; a first dielectric layer (3) over the memory circuit region; a first metallic layer (4) over the first dielectric layer; a contact interconnect between the first metallic layer (4) and the substrate (1); a second dielectric layer (5) on the first metallic (aluminum) layer; a via hole extending through the second dielectric layer to a surface of the second metallic layer; a titanium aluminide layer (206) lining at least a bottom of the via hole; a titanium compound layer (102) formed on the titanium aluminide; a conductive material (103') formed on the titanium compound layer; and a second metallic layer (103) on the second dielectric layer and electrically connected to the plug material.

Harada et al does not teach an antireflecting coating over the aluminum layer.

However, Kanamori teaches in Fig.1(f) the antireflecting coating layer (5) located at between aluminum layer and second dielectric layer. It is common to use a layer of material to suppress reflections from underlying surfaces during photolithography exposure steps. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form the antireflecting coating layer, since antireflecting coating layer suppresses reflections from underlying layers so that the photoresist is not exposed to the reflected light wave, which leads to variation in critical dimensions.

Neither Harada et al nor Kanamori teaches a computer system in which comprises a semiconductor device as teaching by Harada et al as modified by

Kanamori. It would have been obvious to one of ordinary skill in the art to have a processor in computer system since a RAM fabricated on a semiconductor chip communicates with the processor while computer is operating.

4. Claims **33-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al in view of Kanamori, as applied claim **28** above, and further in view of Clayton (US 4,656,605).

Regarding claims **33-36**, Harada et al as modified by Kanamori teaches all claimed structure as claimed in claims 33-40, as explained above in claim 28.

Neither Harada nor Kanamori teaches preformed titanium aluminide layer being volume reduced. However, the term "*preformed titanium aluminide layer being volume reduced*" is process limitation which recites process step to form the structure claimed in 33-36. The process limitations are given no patentable weight in device claim. The final structure of claimed invention is identical to the Harada's device. Therefore, claimed structure is taken to be in the least obvious over Harada.

Neither Harada nor Kanamori teaches a memory module which include a semiconductor device. However, Clayton teaches the memory module comprising (Fig.2):

a substrate comprising a circuit board (31); a plurality of memory chips (10-18) mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprises a random access memory (RAM) fabricated on a

semiconductor substrate which comprising the teaching of Harada; and an edge connector (20) along one edge of the substrate which is wired to said memory circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have module system, since module system includes a plurality of components each storing or reading on binary bit at a time in the semiconductor memory device.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Donghee Kang, Ph.D
December 21, 2001